Amendments to the Specification:

Please amend the specification as follows:

Amend the specification at paragraph at page 8, line 15 to page 9, line 2, as follows:

As an example, FIG. 3 shows the first received strobe signal at node B being 90° out of phase with the received data signal at write block 114. FIG. 4 shows the second received strobe signal at node C being 90° out of phase with the received data signal at write block 126. In FIG. 3, the phase adjusted internal clock signal at node A is 90° out of phase with the received strobe signal at node B. In FIG. 4, the phase adjusted internal clock signal at node A is an arbitrary amount out of phase with the received strobe signal at node C. The arbitrary phase difference in FIG. 4 is expressed as a desired minimum phase difference (for example 90°) + X°, where in X may be for example, 360°. In other embodiments, X might be some other amount such as 270° or 450°. In some embodiments, synchronizers 158 and 164 add phase difference between writing and reading if the phase difference between nodes A and B or A and C gets below the desired minimum amount (in this example 90°) and will remove phase difference if the phase difference gets more than the minimum amount + X (in this example 90° + 360°). Because of the fixed delay between nodes A and B, it may be that synchronizer 158 does not have add or remove phase difference. Although the desired minimum phase difference is mentioned as 90°, other amounts might be used such as 270° (that is, in 1.5 bit cells). <u>As illustrated in FIGS. 3 and 4, 90° corresponds to ½ a bit cell and ¼ cycle.</u> Note that the desired minimum phase difference and the additional delay X do not have to be multiples of 90°.

Amend the specification at paragraph at page 11, lines 6-19, as follows:

Transmitters 104, 144, 138, and 178 are not restricted to any particular circuitry. In some embodiments, transmitters such as transmitter 104 may perform as both a termination and a level translator between chip 30 and chip 20 supply voltages. Referring to FIG. 10, to perform the translation function, the logic power supply (chip 20 Vcc) may be connected to a p-type metal oxide semiconductor field effect transistor (PMOSFET) section of a push-pull transmitter 244 in chip 20,

and drive one-half this supply voltage level. As the transmitters may also serve as terminators, tunable, binary weighted, complementary MOS (CMOS) push-pull transmitters 104 and 244 with linearizing resistors (not shown) may be used. Transmitter 104 receives signals with swings within the Vcc of chip 30 (chip 30 Vcc swings) and transmitter 244 receives signals with swings within the Vcc of chip 20 (chip 20 Vcc swings). The transmitter may implement a slew-rate control function by further segmenting the buffer transistors into four equal subsegments driving in parallel. Delay-line taps may drive these segments to effect a controlled output switching rate, reducing high-frequency content of the channel. The Vccs of chips 20 and 30 may be the same or different. Receivers 246 and 102 are shown. Low voltage swing may be achieved by, for example, replacing the PMOSFET with an n-type MOSFET (NMOSFET). Note that the transistors do not have to be a metal oxide semiconductor type of FETs or even FETs.

Amend the specification at paragraph at page 11, line 20, to page 12, line 12, as follows:

The inventions are not restricted to a particular type of receiver. In some embodiments, receivers 102, 142, 136, and 176 may include the details shown in FIG. 11, but this is not required. Referring to FIG. 11, receiver 102 may subtract the voltage of the outgoing data from transmitter 104 from the voltage on conductor 50-1 to receive the incoming data signal; be capable of operating over a wide range of input common mode levels; maintain high common-mode noise rejection; and provide amplification to convert the received signals to CMOS levels. As shown in the example of FIG. 11, receiver 102 may have three stages. The first stage may be based on a pair of complementary differential amplifiers and provide wide common-mode input range and common-mode noise rejection. The amplifier may perform outbound subtraction by use of a pair of selectable references RefHi and RefLo selected by signals HiSel and LoSel. The first stage (including the following transistors: M1, two M2's, two M3's, two M4's, two M5's, M6, two M7's, and two M8's) may be further divided into four parallel segments to achieve staged, controlled switching between the two references in order to maintain a closely matched relationship with slew-rate controlled outbound data switching. The first stage receives signals Pbias, Nbias, Din, LoSel, and RefHi, and provides signals Doutn, Doutp, Routn, and Toutp. The second stage amplifier (including the following transistors: two M9's, two M10's, two M11's, and two M12's) may

provide gain, common mode restoration, and combine the outputs of the first stage differential amplifiers into a single differential signal. The second stage receives signals Doutn, Doutp, Routn, and Routp. The ~~last stage~~ third stage (including the following transistors: two M13's, two M14's, two M15's, and two M16's) may provide additional gain and convert the differential signal into a single-ended CMOS output at conductor 106. The third stage provides signal RcvOut.